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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,171	06/19/2003	Koji Suzuki	YKI-0132	9732

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,171	SUZUKI, KOJI	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1205, 0206*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/14/05 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzawa et al., U.S. Patent 6,809,339.

Suzawa et al. shows the invention as claimed including a method for manufacturing a thin film transistor, comprising the steps of: forming a semiconductor film 303 above a substrate; forming a gate insulating film 304 to cover the semiconductor film; forming a gate electrode 305,306 on the gate insulating film, wherein the gate electrode comprises a refractory metal; forming a source region and a

drain region 308 in the semiconductor film; and forming an interlayer insulating film 576,578 on the gate electrode, wherein in the formation of the gate electrode, an electrode material layer is layered on the gate insulating film; a mask pattern 307 is formed on the electrode material layer; a first etching process is applied in which the electrode material layer is etched using gas containing fluorine or gas containing a mixture of fluorine and oxygen (see fig. 3A and col. 11-line 64 to col. 12-line 25), and with the mask pattern as a mask to a degree wherein a portion of the electrode material layer remains; and a second etching process is applied in which the electrode material layer is etched using a gas containing a mixture of chlorine and oxygen (see fig. 3C and col. 12-line 55 to col. 13-line 16), in the first etching process, the electrode material layer which uses a refractory metal material is anisotropically etched with a lower ashing with respect to the mask than that in the second etching process, and in the second etching process, the electrode material layer after the first etching process is applied is isotropically etched with a higher ashing with respect to the mask than that in the first etching process (see figs. 3a-3e and col. 11-line 43 to col. 17-line 56).

Concerning claim 25, note that Suzawa et al. also discloses that a first etching process and a second etching process are applied to the electrode material layer with the mask pattern made of a resist material as a mask, wherein in the first etching process, an etching gas having a smaller etching selection ratio between the electrode material layer and the gate insulating film than an etching gas used in the second etching process and having a faster etching rate of the electrode material layer than the etching gas of the second etching process is used, and in the second etching process, a

gate electrode having a tapered shape wherein the side surface is inclined such that the width becomes narrower toward the upper surface is obtained; the electrode material layer after the first etching process is applied is isotropically etched with a higher ashing with respect to the mask than that in the first etching process.

Regarding claim 26, note that both the first and second etching processes are performed in the reaction chamber of an inductively coupled plasma apparatus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa et al., U.S. Patent 6,809,339 in view of Chen et al., U.S. Patent 6,283,131 or Yang et al., U.S. Patent 6,579,809.

Suzawa et al. is applied as above but does not expressly disclose where both the first and second etching processes are performed in the same chamber. Chen et al. discloses performing multiple etch processes involving a gate electrode in the same chamber (see col. 3-lines 46-65). Alternatively, Yang et al. also discloses performing multiple etch processes involving a gate electrode in the same chamber (see col. 2-lines 35-40). In view of these disclosures, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Suzawa et al. so as to perform multiple etching processes in a single chamber as suggested by Chen et al. and Yang et al. because such processes will improve throughput and reduce the possibility of contamination.

Concerning claims 2 and 4, note that the source and drain of Suzawa et al. are formed by implanting through the gate insulating film (see figs. 3B and 3C).

Regarding claims 3-4, note that the gate insulating film can be silicon oxide or silicon nitride (see col. 19-lines 12-17),

With respect to claims 8-9 and 12-13, note that in Suzawa et al., after a gate insulating film is formed on the semiconductor film, the electrode material layer is formed on the gate insulating film and after a semiconductor film is formed above the substrate, the electrode material layer is formed above the semiconductor film.

Concerning claim 5, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum volume ratio of fluorine and oxygen gas in the first etching process based upon a variety of factors including the desired profile of the electrode and such a limitation would not lend patentability to the instant application absent a showing of unexpected results. Furthermore, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. (see In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)).

Claims 10, 15, 21-23, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa et al., U.S. Patent 6,809,339 in view of Chen et al., U.S. Patent 6,283,131 or Yang et al., U.S. Patent 6,579,809 as applied to claims 1-9 and 14 above, and further in view of Admitted prior art.

Suzawa et al., Chen et al., and Yang et al. are applied as above but do not expressly disclose forming the electrode prior to forming the semiconductor film or forming the gate electrode as a single layer refractory metal film. Admitted prior art discloses forming the electrode prior to forming the semiconductor film, known as a bottom gate TFT (see page 1 of the specification, lines 12-13), and forming the gate electrode of a single layer refractory metal film (see fig. 1B of the specification). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Suzawa et al. modified by Chen

et al. or Yang et al. so as to have the gate electrode constructed of a single layer refractory metal film or as a bottom gate TFT because such constructions are commonly used in thin film transistor technology in order to drive liquid crystal display devices.

Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa et al., U.S. Patent 6,809,339 in view of Admitted prior art.

Suzawa et al. is applied as above but does not expressly disclose forming the gate electrode of a single layer refractory metal film. Admitted prior art discloses forming the gate electrode of a single layer refractory metal film (see fig. 1B of the specification). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Suzawa et al. modified by Chen et al. or Yang et al. so as to have the gate electrode constructed of a single layer refractory metal film because such a construction is commonly used in thin film transistor technology in order to drive liquid crystal display devices.

Claims 1-6, 21-22, and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figures IA-IB and their description in pages 1-4 of the instant application in view of Fukuda (U.S. Patent No. 5,880,035) and further in view of Chen et al., U.S. Patent 6,283,131 or Yang et al., U.S. Patent 6,579,809.

With regard to Claim 1, Applicant's admitted prior art discloses a method for manufacturing a thin-film transistor, comprising the steps of: forming a semiconductor

film (23) above a substrate (21), forming a gate insulating film (24) to cover the semiconductor film, forming a gate electrode (25) on the gate insulating film (24), wherein the gate electrode (25) comprises a refractory metal (Mo) (see page I , lines 23-25 of the instant application) forming a source region (23s) and a drain region (23d) in the semiconductor film and forming an interlayer insulating film (26) on the gate electrode (25), wherein in the formation of the gate electrode (25), an electrode material layer is layered on the gate insulating film (24); a mask pattem is formed on the electrode material layer (see page 3, lines 1-3 of the instant application; an etching process is applied in which the electrode material layer is etched using gas containing fluorine or gas containing a mixture of fluorine and oxygen (see page 3, lines 3-6 of the instant application), and with the mask pattem as a mask to a degree wherein a portion of the electrode material layer remains.

Applicant's admitted prior art fails to disclose the claimed second etching process using a gas containing a mixture of chlorine and oxygen and performing the first and second etching processes in the same chamber. However, Fukuda discloses a dry-etching method for a gate electrode comprising layers (2, 3) wherein layer (2) comprises a refractory metal (column 5, lines 58-60). The dry-etching method includes a first etching step wherein the gas used in said first etch step is SF6 and a second etch step wherein the gas used is C12/O2 (see column 3, lines 28-33 and column 6, lines 1-21 and 41-42). Therefore, it would have been obvious modification to one of ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed second etching process, which uses a gas

containing a mixture of chlorine and oxygen, as suggested by Fukuda, in order to provide a dry-etching method that enables higher productivity and a higher yield without damaging the substrate or a gate oxide film (column 2, lines 45-50).

With respect to the etching processes being performed in the same chamber, Chen et al. discloses performing multiple etch processes involving a gate electrode in the same chamber (see col. 3-lines 46-65). Alternatively, Yang et al. also discloses performing multiple etch processes involving a gate electrode in the same chamber (see col. 2-lines 35-40). In view of these disclosures, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of the admitted prior art modified by Fukuda et al. so as to perform multiple etching processes in a single chamber as suggested by Chen et al. and Yang et al. because such processes will improve throughput and reduce the possibility of contamination.

With regard to Claim 2, Applicant's admitted prior art discloses that the source region (23s) and the drain region (23d) are formed by, doping impurities into the semiconductor film (23) through the gate insulating film (24) (see page 1, lines 25-28 of the instant application).

With regard to Claim 3, Applicant's admitted prior art discloses a gate insulating film (24) that is obtained by layering a SiN film and a SiO2 film or by forming one of the SiN film and SiO2 film (see page 1, line 22 of the instant application).

With regard to Claim 4, Applicant's admitted prior art discloses a source region (23s) and a drain region (23d) formed by doping impurities into the semiconductor film (23) through the gate.

Concerning claim 5, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum volume ratio of fluorine and oxygen gas in the first etching process based upon a variety of factors including the desired profile of the electrode and such a limitation would not lend patentability to the instant application absent a showing of unexpected results. Furthermore, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. (see In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)).

Claims 7-15, 23, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figures IA-IB and their description in pages 1-4 of the instant application in view of Fukuda (U.S. Patent No. 5,880,035) and further in view of Chen et al., U.S. Patent 6,283,131 or Yang et al., U.S. Patent 6,579,809 as applied to claims 1-6 and 21-22 above, and further in view of Paranjpe et al. (U.S. Patent No. 5,580,385).

With regard to Claim 7, Applicant's admitted prior art, Fukuda, Chen et al., and Yang et al. essentially disclose the claimed invention, but fail to disclose the claimed inductively-coupled plasma apparatus. However, Paranjpe discloses a method for incorporating an inductively coupled plasma source in a plasma processing chamber, wherein the inductively-coupled plasma source comprises an antenna (14) powered by at least one RF power supply (40) through at leastone RF matching network (42) and a

plasma-formation region (See figure 1). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed inductively-coupled plasma apparatus instead of the ECR plasma etching system of Fukuda, in order to provide a plasma processing chamber with a source that has substantially lower instrinsic plasma potentials and achieve substantially higher ionization efficiency (column 1, lines 31-40) and operates over a pressure range that is more compatible with process requirements (column 1, lines 48-50).

With regard to Claim 8, Applicant's admitted prior art discloses a semiconductor film (23) that is formed above a substrate (21) and an electrode material (25) that is formed above the semiconductor film (23) (see figures IA-IB and page 1 , lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 9, Applicant's admitted prior art discloses a gate insulating film (24) that is formed on a semiconductor film (23) and an electrode material layer (25) formed on the gate insulating film (24) (see figures IA-IB and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 10, Applicant's admitted prior art discloses a process step of forming a gate electrode (25), wherein the gate electrode has a tapered shape (see figures IA-IB and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

Response to Arguments

Applicant's arguments with respect to claims 1-15 and 21-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

March 4, 2006